REMARKS

By this amendment, claims 1 and 15 have been amended. Claims 3, 11-15, and 17 have been withdrawn. New claims 42-43 have been added. It should be noted that claims 1 and 15 are generic to all species according to the Examiner's Election of Species Requirement. Claims 1-5, 8-18, 20-21, and 41-43 are pending in the application. Applicants reserve the right to pursue the original claims and other claims in this and other applications.

Claims 1-2, 4-5, 7-9, 15, 17, 19, 20, and 40-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrill et al. (US 6,512,544) in view of Sauer (US 6,320,616). This rejection is respectfully traversed. In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Neither Merrill et al. nor Sauer, even when considered in combination, teaches or suggests all limitations of independent claims 1 and 15.

Claim 1 recites a method of processing pixel signals comprising, *inter alia*, "clamping a pixel readout line to a voltage level less than a voltage corresponding to a pixel signal; subsequently coupling the pixel readout line to an output of a source-follower transistor and reading out the pixel signal onto the pixel readout line; [and] subsequently clamping a capacitive storage node in a pixel signal processing circuit to a voltage less than a voltage corresponding to the pixel signal appearing on the pixel readout line" (emphasis added). Claim 15 recites similar limitations for an imager. Applicants respectfully submit that Merrill et al. and Sauer, even when combined, do not teach or suggest these limitations.

To the contrary, Sauer teaches that the highest possible value of the Col_Read(x) line is 3.801V, and the voltage is lowered by the pixel signal readout. Col. 8, ln. 18-19. Activation of clamp line CL, "causes the APS reference voltage of 3.801 V to be applied to node 157." Col. 7, ln. 38-39 (emphasis added). "The voltage (3.801 V) on the Col_Read(x) line at this stage may be referred to as the APS reference voltage, since it serves as a reference to measure the voltage difference which will be caused when the photo signal charge is transferred to FD node 115." Col. 7, ln. 17-21.

Although the Office Action claims that Sauer teaches "clamping the capacitive storage node (157) to a voltage less than a voltage correspond[ing] to the pixel signal appearing on the pixel readout line," Sauer actually teaches that "[r]esetting the voltage at FD node 115 in this manner may be referred to as preconditioning or precharging the node, since the node is thereby made receptive to having charge transferred from the photodetector 116." Col. 6, ln. 66 – Col. 7, ln. 2 (emphasis added). Sauer teaches that "any charge stored during the integration period on photodetector 116 ... pulls down voltage at FD node 115 ... proportional to the intensity of light received by the pixel." Col. 7, ln. 62-67 (emphasis added). Then, "the voltage at node 157 falls by 1 V, which change is indicative of the amount of light sensed." Col. 8, ln. 23-24 (emphasis added). Therefore, the pixel signal is lower than the voltage to which the capacitive node 157 was previously clamped.

Applicants respectfully submit that Sauer does not disclose, teach, or suggest "clamping a pixel readout line to a voltage level less than a voltage corresponding to a pixel signal; subsequently coupling the pixel readout line to an output of a source-follower transistor and reading out the pixel signal onto the pixel readout line; [and] subsequently clamping a capacitive storage node in a pixel signal processing circuit to a voltage less than

a voltage corresponding to the pixel signal appearing on the pixel readout line," as recited in claims 1 and 15. Nor does Merrill et al. teach or suggest these limitations. Thus, Merrill et al. does not remedy the deficiencies of Sauer.

The Supreme Court recently held in *KSR Int'l Co. v. Teleflex Inc.* that "the [Graham] factors continue to define the inquiry that controls" a finding of obviousness and reiterated that a "patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." 127 S.Ct. 1727, 1734 (U.S. 2007). The Graham factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966).

Since Merrill et al. and Sauer do not teach or suggest all of the limitations of claims 1 and 15, claims 1 and 15 are not obvious over the cited references. Claims 2, 4-5, 7-9, 17, 19, 20, and 40-41 depend, respectively, from independent claims 1 and 15, and are patentable at least for the reasons mentioned above, and on their own merits. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 1-2, 4-5, 7-9, 15, 17, 19, 20, and 40-41 be withdrawn and the claims allowed.

In addition, new claims 42-43, which are dependent, respectively, on claims 1 and 15, recite that "the capacitive storage node comprising a binary scaled capacitor network." Sauer teaches in FIG. 1 only the individual capacitors C1, C2, and C5, but is silent with respect to any values or respective values for the capacitors. Applicants respectfully submit that Sauer does not disclose, teach, or suggest a capacitive storage node comprising a binary scaled capacitor network, as recited in claims 1 and 15. Nor does Merrill et al.

teach or suggest these limitations. Thus, Merrill et al. does not remedy the deficiencies of Sauer.

In view of the above, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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